REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-21 are now in the application. Claims 1, 6, 9, 10, and 12 have been amended. Dependent claims 18-21 have been added.

Support for the new claims can be found on page 13, last paragraph of the instant specification.

In item 1 on page 2 of the above-identified Office Action, claims 1-5, 9-12, 14, and 15 have been rejected as being unpatentable over Chambers (U.S. 6,047,365) in view of Fitch et al. (U.S. 5,056,060) (hereinafter "Fitch") under 35 U.S.C. § 103(a).

In item 8 on page 4 of the above-identified Office Action, claims 6, 7, and 8 have been rejected as being unpatentable over Chambers in view of Fitch and further in view of Arnold et al. (U.S. 4,558,176) (hereinafter "Arnold") under 35 U.S.C. § 103(a).

In item 10 on page 5 of the above-identified Office Action, claims 13, 16, and 17 have been rejected as being unpatentable

over Chambers in view of Fitch and further in view of Wright et al. (U.S. 4,802,218) (hereinafter "Wright") under 35 U.S.C. § 103(a).

The rejections have been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 5, line 37 to line 2, page 6; page 6, second paragraph; page 8, second paragraph; page 13, third paragraph of the specification of the instant application; and in the original claims of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a microprocessor circuit, comprising:

at least one control unit;

at least one memory for free programming with at least one program having functions, the memory connected to the control unit;

a register bank having registers, the register bank connected to the control unit;

an auxiliary register storing a number of bits, each of the bits being associated with one of the registers of the register bank and indicating whether a respective one of the registers contains a value different from a logical "0", the auxiliary register connected to at least one of the control unit or the register bank, and

a stack buffer-storing data of at least one of the auxiliary register or the registers of the register bank, the stack connected to at least one of said control unit, the register bank, or the auxiliary register.

Chambers discloses optimizing sample fetching in a peripheral component interconnect environment including generating a first sample page base address corresponding to a first part of a first address received from a digital signal processor. The Examiner alleges that Chambers shows a microprocessor circuit comprising a stack [306] for buffer-storing data. However, no support is found for this statement in Chambers. While a stack may be implemented in the system memory of Chambers, Chambers shows a special addressing scheme of memory cells, either as first-in-first-out (FIFO) or first-in-last-out (FILO). Chambers does not disclose anything about a stack as set forth in the claims of the instant application. The identification by the Examiner in item 2(b) of the Office

Action of the wave table sample page [306] as a stack is incorrect because it not only lacks the features of a stack, but also because the wave table sample page [306] previously has already been identified by the Examiner as memory for free programming. The same component cannot be used for two specifically claimed different features. Therefore, claim 1 is believed to be patentably distinct with respect to Chambers.

Claim 1 also recites the feature that the stack buffer stores data of at least one of the auxiliary register and the registers of the register bank. There is no disclosure or suggestion in Chambers to store the data in the valid bit register array [310] in a stack.

Fitch discloses a printed circuit board card having a self-configuring memory system for allocation of reserved memory space among expansion cards in which the printed card fits into a slot and makes electrical connections with a cooperating terminals in the slot. The slot is located on the main circuit board of a personal computer system. Fitch doe snot make up for the deficiencies of Chambers. Fitch doe snot storing the data in a valid bit register array in a stack as recited in claim 1.

The references do not show "a stack buffer-storing data of at least one of said auxiliary register or said registers of said register bank, said stack connected to at least one of said control unit, said register bank, or said auxiliary register" as recited in claim 1 of the instant application.

Claim 12 recites a method for operating a microprocessor circuit according to the present invention including storing data of the auxiliary register and/or the register of the register bank in the stack. At least for the same reasons discussed above relative to claim 1, claim 12 also is deemed patentably distinct over the applied prior art. Further, claim 12 recites the feature of storing data from the stack in the auxiliary register and/or the register bank. This feature is not shown in the cited prior art.

Arnold discloses a computer system for inhibiting unauthorized copying, usage, and automated cracking of protected software. The system executes protected programs which are protected by encapsulation and/or encryption and includes an arrangement that detects and inhibits automated cracking of protected programs unauthorized. Arnold doe snot make up for the deficiencies of Chambers and/r Fitch.

Wright discloses an automated transaction system using a card maintaining an account balance and a terminal for dispensing an article of value and debiting the card's balance. Wright doe snot make up for the deficiencies of Chambers and Fitch.

The references do not show "storing data being stored in at least one of the auxiliary register or the registers of the register bank in the stack, or storing data which is stored in the stack in at least one of the auxiliary register or the registers of the register bank" as recited in claim 12 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 12. Claims 1 and 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 12.

In view of the foregoing, reconsideration and allowance of claims 1-21 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

If an extension if time for this paper is required, petition for extension is herewith made.

Enclosed is payment in the amount of $50.00 for a single claim in excess twenty claims filed with the original application. Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

F. Donald Paris (24,054)

FDP/bb

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101